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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 10/606,283

Confirmation No.: 3304

In re Application of:

Noriko SHINOMIYA

Group Art Unit: 2825

Filed: June 26, 2003

Examiner: Unassigned

For: SEMICONDUCTOR INTEGRATED CIRCUIT DESIGNING APPARATUS,
SEMICONDUCTOR INTEGRATED CIRCUIT DESIGNING METHOD,
SEMICONDUCTOR INTEGRATED CIRCUIT MANUFACTURING METHOD,
AND READABLE RECORDING MEDIA

STATUS INQUIRY LETTER


Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It would be appreciated if you would indicate the status of the above-identified application below, including an indication as to when the next communication can be expected, and return this sheet to the undersigned.

Respectfully submitted,
STEPTOE & JOHNSON LLP

May 26, 2005
Date


Roger W. Parkhurst
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Attorney Docket No.: 28951.1165 (HYAE:165)
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